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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,162	12/15/2003	Ji Yong Park	0095.1054	2087
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EXAMINER KIM, JAY C				
ART UNIT 2815		PAPER NUMBER		
NOTIFICATION DATE 07/23/2010		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptomail@smiplaw.com

Office Action Summary

Application No.

10/734,162

Applicant(s)

PARK ET AL.

Examiner

JAY C. KIM

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 May 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-7 and 9-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-7 and 9-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

This Office Action is in response to RCE filed May 14, 2010.

Claim Objections

1. Claims 1, 6 and 7 are objected to because of the following informalities:

On lines 6 and 8 of claim 1, "the" before "primary crystal grain boundaries" should be removed to avoid indefiniteness.

In claim 6, "the LDD or offset region" on line 8 and "the LDD region or offset region" on line 9 should be replaced by "an LDD or offset region" or "the LDD or offset regions", because an LDD region or offset region is formed at respective opposite sides of the channel region.

On lines 4-5 of claim 7, ", the offset regions having no doping" should be removed and the limitation is considered a typographical error in the below prior art rejection, because Applicants stated that "[H]owever, in order to further clarify this matter and not for purposes related to patentability, Applicants have amended independent claims 1 and 7 to remove the term having no doping" on page 7 of REMARKS filed May 14, 2010", Applicants deleted limitation "having no doping" from claim 1, and otherwise the Examiner would maintain 35 USC 112, second paragraph, rejection of claim 7 provided in Final Office Action mailed January 14, 2010, and objection to Drawings stated below in *Response to Arguments*.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 6, 7 and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Oka et al. (US 6,184,541).

Regarding claim 6, Oka et al. disclose a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42), source and drain regions (5) (col. 3, lines 39-40) respectively formed at opposite sides (left and right sides) of the channel region (8), a lightly doped drain (LDD) region or offset region (portion of region 4 having a width d in Fig. 1(b)) (col. 3, lines 60-66, and col. 4, lines 63-66) respectively formed at opposite sides (left and right sides) of the channel region (8) and between the source and drain regions (5), and a plurality of primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are positioned in the channel, source and drain regions (8 and 5) but not positioned in the LDD or offset regions (portions of regions 4 having a width d in Fig. 1(b)), and wherein a width (d) of the LDD or offset regions is less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain

boundary in region 4 on the right shown in Fig. 1(a)) because the LDD or offset regions are formed between two adjoining primary crystal grain boundaries.

Regarding claim 7, Oka et al. disclose a flat panel display device (col. 2, lines 27-29) comprising a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42), offset regions or *off-center regions* (portions of regions 4 having a width d in Fig. 1(b)) (col. 3, lines 38-39) formed at opposite sides (left and right sides) of the channel region (8), (for the limitation "the offset regions having no doping", see *Claim Objections* above), source and drain regions (5) (col. 3, lines 39-40) respectively formed at outer sides of the offset regions, and a plurality of primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are not positioned in the offset regions (portions of regions 4 having a width d in Fig. 1(b)), and wherein a width of the offset regions (d) is smaller than a distance between the primary crystal grain boundaries (2) because the offset regions are formed between two primary crystal grain boundaries, for example, one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain boundary in region 4 on the right shown in Fig. 1(a).

Regarding claim 9, Oka et al. disclose the flat panel display device according to claim 7.

The limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS) method" is merely a product-by-process limitation that does not

structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claim 10, Oka et al. further disclose for the flat panel display device according to claim 7 that the thin film transistor is used in an LCD device (col. 2, lines 27-29).

Regarding claim 11, Oka et al. further disclose for the flat panel display device according to claim 7 that the primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) are substantially perpendicular to a current direction (left-to-right or right-to-left direction) between the source and drain regions (5) of the thin film transistor.

Regarding claim 12, Oka et al. disclose a flat panel display device (col. 2, lines 27-29) comprising a thin film transistor (Figs. 1(a), 1(b) and 3(g)) comprising a lightly doped drain (LDD) region or offset region (portion of region 4 having a width d on the right side) (col. 3, lines 60-66, and col. 4, lines 63-66), and a plurality of primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are positioned in channel, source and drain regions (8 and 5) (col. 3, lines 42 and 39-40) but not positioned in the LDD or offset region (portion of region 4 having a width d on the right side), and wherein

a width (d) of the LDD region or offset region is less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain boundary in region 4 on the right shown in Fig. 1(a)) because the LDD or offset region is formed between two adjoining primary crystal grain boundaries.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka et al. (US 6,184,541).

Regarding claim 1, Oka et al. disclose a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42) having a plurality of crystal grain boundaries (2) (col. 3, lines 36-37), source and drain regions (5) (col. 3, lines 39-40) respectively formed at opposite ends (left and right ends) of the channel region (8), and offset regions or *off-center regions* (portions of regions 4 having a width d in Fig. 1(b)) (col. 3, lines 38-39) formed between the source and drain regions (5) and the channel region (8), wherein the thin film transistor is formed so that primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) of a polysilicon

substrate (3) (col. 3, line 36) are not positioned in the offset regions (portions of regions 4 having a width d in Fig. 1(b)).

Oka et al. differ from the claimed invention by not showing that a width of each one of the offset regions is smaller than a distance between primary crystal grain boundaries formed in the channel region.

Oka et al. further disclose that the grain size of the polysilicon substrate (16 in Fig. 3(b)) is as fine as $1.0 \pm 0.5 \mu\text{m}$ and the polysilicon substrate itself has high homogeneity (col. 4, lines 40-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a width of each one of the offset regions (d) may be smaller than a distance between primary crystal grain boundaries formed in the channel region, because d is smaller than a lateral grain size of polysilicon grains in which an offset region is formed, and the width of each one of the offset regions (d) may be smaller than a distance between primary crystal grain boundaries (distance between nearest neighboring primary crystal grain boundaries, or distance between next nearest neighboring primary crystal grain boundaries) formed in the channel region when the grain size of the polysilicon substrate is substantially uniform.

Regarding claim 3, Oka et al. disclose the thin film transistor according to claim 1.

The limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS) method" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a

product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claim 4, Oka et al. further disclose for the thin film transistor according to claim 1 that the thin film transistor is used in an LCD device (col. 2, lines 27-29).

Regarding claim 5, Oka et al. further disclose for the thin film transistor according to claim 1 that the primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) are substantially perpendicular to a current direction (left-to-right or right-to-left direction) between the source and drain regions (5) of the thin film transistor.

Response to Amendment

6. The Proposed Declaration under 37 CFR 1.132 filed May 14, 2010 is insufficient to overcome the rejection of claims 1, 6, 7 and 12 based upon 35 USC 102(b) over Oka et al. as set forth in the last Office action because: (1) Applicants recite "offset region(s)" in the context of "a lightly doped drain (LDD) region or offset region" in claims 6 and 12, and Dictionary.com defines "offset" as "placed away from a center line" or "off-center". Therefore, an LDD region having a width d in Fig. 1(b) of Oka et al. may be referred to as an offset region or *an off-center region* relative to the channel region unless Applicants specifically claim a structure or position of the offset region. (2) Applicants do not specifically claim a structure or position of the LDD region or offset region, that the recited width is "a general length of the LDD region" or that the recited LDD region or offset region is a whole LDD region or offset region in physical contact with the

channel region and the source/drain region. Applicants' definition of an LDD region or offset region is unduly narrow without specifically claiming a structure or position of the LDD region or offset region. A portion of region 4 having a width d in Fig. 1(b) of Oka et al. may be referred to as an LDD region or offset region, while a whole region 4 may also be referred to as an LDD region or offset region, because both of them have distinct structures distinguished from surroundings. In the former case, the rest of region 4 adjacent to the portion of region 4 having a width d may be referred to as another LDD region or offset region. (3) Further, see the responses below.

Response to Arguments

7. Applicants' arguments filed May 14, 2010 have been fully considered but they are not persuasive.

Applicants' arguments that "three exemplary devices are disclosed" and "the specification discloses three examples, and claim 1 refers to two of the exemplary devices, including the LDD region or the offset region" are not persuasive, especially because Applicants did not originally disclose a width or position of an offset region and that the LDD regions II shown in Figs. 5 and 6 of current Application can be replaced by offset regions having the same dimensions and having no doping. However, Applicants' arguments regarding Objection to the Drawings and Rejections under 35 USC 112, first paragraph, are persuasive *only* in a sense that the recited "offset region(s)" is(are) interpreted to be *equivalent* to the LDD region(s) shown in Figs. 5 and 6 of current Application, because (1) Applicants did not originally disclose that the LDD regions II of current Application can be *wholly* replaced by offset regions having the same

dimensions and having no doping, (2) Applicants did not originally disclose where the offset regions are provided, i.e. closer to the source/drain regions or closer to the channel region relative to the LDD regions?, and (3) Applicants originally disclosed that a width of an LDD region is smaller than a distance between primary crystal grain boundaries, but did not originally disclose that a width of an offset region is smaller than a distance between primary crystal grain boundaries. Rather, Applicants originally disclosed that "furthermore, off current, that is, leakage current, can be reduced in a thin film transistor by adding an LDD region to the offset region through low density ion doping of impurities (emphasis added)" in paragraph [0028], which suggests that an LDD region and an offset region are separate and distinct elements, not interchangeable elements as Applicants attempt to suggest. Therefore, one of ordinary skill in the art would recognize that Applicants originally disclosed (1) a thin film transistor having LDD regions II as shown in Figs. 5 and 6 of current Application, and (2) another thin film transistor having LDD regions and offset regions. Therefore, previously presented limitation "offset region having no doping" would require Drawings, and previously presented limitation that "a width of the offset region" having no doping "is smaller than a distance between primary crystal grain boundaries" may have failed to comply with the written description requirement.

Applicants argue that "accordingly, region II illustrated in FIGS. 5 and 6 can be either an LDD region or an offset region", and that "in other words, the LDD region can be replaced by an offset region and vice versa". This was not disclosed in original disclosure. See the above responses.

Applicants argue that "however, Applicants respectfully assert that nowhere in the specification does Oka teach or suggest offset regions". (1) Applicants do not specifically claim what "offset regions" refer to. The argument above is based on importing claim limitations from the specification, which is improper according to MPEP 2111.01. (2) Dictionary.com defines "offset" as "placed away from a center line" or "off-center". Therefore, an LDD region having a width d in Fig. 1(b) of Oka et al. may be referred to as an offset region or *an off-center region* relative to the channel region unless Applicants specifically claim a structure or position of the offset region.

Applicants argue that "regarding the rejection of independent claims 6, 7 and 12 it is noted that these claims recite some substantially similar features as claim 1, such as the offset regions". Independent claims 6 and 12 are completely different in scope from independent claims 1 and 7 in that a lightly doped drain (LDD) region, which may or may not be the same with the offset region, is recited in claims 6 and 12.

Applicants argue that "however, Applicants note that 'd' is an effective length of the LDD region which is different from a general length of the LDD region", that "one of ordinary skill in the art uses the term 'length of the LDD region' to refer to the general length of the LDD region", and that "thus, Oka does not disclose that "a width of the LDD region or offset regions is less than a distance between two adjoining primary crystal grain boundaries". (1) Applicants do not specifically claim a structure or position of the LDD region, or that the recited LDD region is a whole LDD region in direct contact with the channel region and the source/drain region. (2) It is not clear what Applicants suggest by "a general length of the LDD region", and Applicants do not specifically claim

a general length of an LDD region. (3) A portion of region 4 having a width d in Fig. 1(b) of Oka et al. may be referred to as an LDD region, while a whole region 4 may also be referred to as an LDD region, because both of them have distinct structures distinguished from surroundings. In the former case, the rest of region 4 adjacent to the portion of region 4 having a width d may be referred to as another LDD region, which is not precluded in claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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